IN THE CLAIMS

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently Amended) An increasing monotonic counter over n bits formed as an integrated circuit, comprising:

an assembly of 2^{n+1}-(n+2) irreversible counting cells distributed in at least n groups of 2^p-1 counting cells, where p designates [[the]] a group rank; and

at least n-1 parity calculators, each calculator providing a bit of rank p, increasing from [[the]] a most significant bit of [[the]] a result count, taking into account [[the]] states of the cells counting of the group of same rank.

2. (Currently Amended) The counter of claim 1, wherein the most significant bit is directly provided by [[the]] a single cell of [[the]] a group of rank P=1.

3. (Currently Amended) The counter of claim 1, comprising n calculators, the most significant bit being provided by [[the]] a calculator taking into account the state of [[the]] a single counting cell of the group of rank P=1.

4. (Previously Presented) The counter of claim 1, wherein each counting cell is formed of a one-time programming memory cell, a storage element of which is formed of at least one polysilicon resistor, programmable by irreversible decrease in its value.

5. (Currently Amended) A method for controlling ~~the counter of claim 1,~~ an increasing monotonic counter over n bits formed as the integrated circuit including an assembly of 2^{n+1}-(n+2) irreversible counting cells distributed in at least n groups of 2^p-1 counting cells, where p designates a group rank, and at least n-1 parity calculators, each calculator providing a bit of rank p, increasing from a most significant bit of a result count, taking into account states of the cells counting of the group of same rank, the method comprising causing a programming of a counting cell of a group of lower rank each time the parity ~~controller~~ calculator of a group of

immediately higher rank detects a parity.

6. (Original) The method of claim 5, implemented by a state machine in wired logic.

7. (Original) The method of claim 5, implemented by a microcontroller.